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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/980,974	03/06/2002	Karsten Jensen	1406/24	3607

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/980,974	JENSEN ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) __ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Stallings, William, "Computer Organization and Architecture", 1996, Prentice-Hall, Inc., 4th edition, pages 9, 52, and 361-368 , (hereafter referred to as Stallings).

Referring to claim 1, Stallings discloses, as claimed, a method for branching when a program is executed by a processor (see Fig. 3.2), where the program is stored in a program memory (the portion of Memory storing instruction, see Fig. 3.2) , and a variable memory (the portion of Memory storing Data, see Fig. 3.2) and a table memory (the other portion of Memory storing Data, see Fig. 3.2) for storing fixed values are provided, the

processor executing the following steps within a single jump instruction (note this is the situation when a jump instruction is executed in the Stallings's, and see also page 367, lines 28-30, regarding both indirect addressing and indexing are provided, and it is possible to employ both in the same instruction):

a) addressing (by the address A, see page 367, lines 39-40) a first memory cell (the memory cell saves (A) value, see page 367, lines 28-41, when the postindexing addressing mode is used wherein EA =(A) + (R)) in the variable memory (the portion of Memory storing Data, see Fig. 3.2).

b) addressing a second memory cell (at the address EA saving the address value (EA) see indirect addressing mode in Fig. 10.1 or page 364, lines 12-36) in the variable memory (the portion of Memory storing Data, see Fig. 3.2) on the basis of the content ((A) value since EA =(A) + (R))of the first memory cell addressed in step a), and further parameters ((R) value in the index register since EA =(A) + (R)),

c) addressing a third memory cell (at the address (EA) saving the address value ((EA)) see indirect addressing mode in Fig. 10.1 or page 364, lines 12-36) in the table memory on the basis of the content (the address value (EA), see indirect

addressing mode in Fig. 10.1 or page 364, lines 12-36) of the second memory cell, addressed in step b), and

d) branching execution to a program address (at address ((EA)) of the program memory (the portion of Memory storing instruction, see Fig. 3.2), note this is in the situation when the address (EA) is used to reference the variable memory cell saving the address value of ((EA))) which is stored in the third memory cell in the table memory (the other portion of Memory storing Data, see Fig. 3.2) which was addressed in step c).

As to claim 2, Stallings also discloses: addressing the second memory cell in the variable memory is addressed (at the address EA =(A) + (R)) by the result of an instruction which processes the content of the first memory cell (the memory cell saves (A) value) in the variable memory and further parameters ((R) value in the index register since EA =(A) + (R)).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this

> title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stallings in view of Tanenbaum, Andrew S., "Modern Operating Systems", 1992, Prentice-Hall, Inc., pages 128-130, (hereafter referred to as Tanenbaum)

Stallings discloses the claimed invention except for: addressing the variable memory is addressed using a first bit length a, and addressing the table memory using a second bit length b, the first bit length a and the second bit length b being of different size.

Stallings shows, as set forth above, addressing a program memory (the portion of Memory storing instruction, see Fig. 3.2), a variable memory (the portion of Memory storing Data, see Fig. 3.2) and a table memory (the other portion of Memory storing Data, see Fig. 3.2). The variable memory data may bump into the data in program memory or table memory during the execution of process in the Stallings's system (see Fig. 3-35 in Tanenbaum).

Tanenbaum shows that it is well know in the art to address separate segments (see Fig. 3-36) for storing different data in

order to allow each data in its memory segment to grow or shrink independently of the other data. Further, it is well known in the art that the bit length used for addressing a memory is related to the size of the memory in order to save the address bits.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Stallings's system to comprise addressing the variable memory is addressed using a first bit length a, and addressing the table memory using a second bit length b, the first bit length a and the second bit length b being of different size, as taught by Tanenbaum, in order to prevent the variable memory data from bumping into the data in program memory or table memory and to save the address bits used for referencing the memories in the Stallings's system.

Response to Amendment

5. Applicant's arguments filed 12/23/04 have been fully considered but they are not deemed to be persuasive.

Regarding the specification problems, Examiner agrees with Applicant that Applicant's preliminary amendment mailed 3/6/02 has overcome the objection.

Applicants argue that "Stallings does not teach a method **executing steps a-d within a single jump instruction as required** by Claim 1" (page 4, lines 18-20); and "Stallings teaches **postindexing, autoindexing, and indirect addressing modes and it is well known to those of ordinary skill in the relevant art the each addressing instruction must be loaded, decoded, and** executed according to the Von Neuman memory configuration model" **(page 4, last two and page 5, lines 1-3).** Examiner disagrees with Applicants. As set forth in the art rejections above, Stallings discloses, as claimed, a method for branching when a program is executed by a processor (see Fig. 3.2), the processor executing the following steps (a-d) within a single jump instruction (note this is the situation when a jump instruction is executed in the Stallings's system, and see also page 367, lines 28-30, regarding both indirect addressing and indexing are provided, and it is possible to employ both in the same

instruction). Further, the addressing modes can be used in such as Pentium or PowerPC system.

Regarding claim 3, Applicants argue that "Nowhere does **Tanenbaum disclose or suggest executing steps for addressing different memory cells within a single jump instruction" (page 7, lines 14-15).** Examiner disagrees with Applicants. Again, as set forth in the art rejections above, Stallings discloses, as claimed, a method for branching when a program is executed by a processor (see Fig. 3.2), the processor executing the following steps (a-d) within a single jump instruction (note this is the situation when a jump instruction is executed in the Stallings's system, and see also page 367, lines 28-30, regarding both indirect addressing and indexing are provided, and it is possible to employ both in the same instruction). Tanenbaum is cited to show that it is well know in the art to address separate segments (see Fig. 3-36) for storing different data in order to allow each data in its memory segment to grow or shrink independently of the other data. Stallings in view of Tanenbaum teaches the claimed invention described in claim 3.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful,

the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

8. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
February 9, 2005